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- [1] R. E. Blahut
Theory and Practice of Error Control Codes. Reading, MA: Addison-Wesley, 1983.

PROCEEDINGS ARTICLE:

- [2] T. Fichna, M. Gartner, F. Gliem, and F. Rombeck
Fault-tolerance of spaceborne semiconductor mass memories.
In *Twenty-Eighth Annual International Symposium on Fault-Tolerant Computing, Digest of Papers*, 1998, 408–413.

BOOK:

- [3] P. K. Lala
Fault Tolerant and Fault Testable Hardware Design. Englewood Cliffs, NJ: Prentice-Hall, 1985.

WEB SITE:

- [4] National Semiconductors Inc.
Homepage: <http://www.national.com>.

PROCEEDINGS ARTICLE:

- [5] C. Paar and M. Rosner
Comparison of arithmetic architectures for reed-solomon decoders in reconfigurable hardware.
In *Proceedings of the Symposium on Field-Programmable Custom Computing Machines*, Apr. 1997, 219–225.

JOURNAL ARTICLE:

- [6] N. R. Saxena and E. J. McCluskey
Parallel signature analysis design with bounds on aliasing.
IEEE Transactions on Computers, **46**, 4 (Apr. 1997), 425–438.
- [7] C. I. Underwood and M. K. Oldfield
Observations on the reliability of cots-device-based solid state data recorders operating in low-Earth orbit.
IEEE Transactions on Nuclear Science, **47**, 4 (June 2000), 647–653.

WEB SITE:

- [8] Xilinx Inc.
Homepage: <http://www.xilinx.com>.